This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original) A semiconductor integrated circuit, comprising

an amplifier circuit of AM broadcast signals having a first P channel MOSFET for amplifying AM broadcast signals and a second P channel MOSFET cascade-connected to the first P channel MOSFET; and

a CMOS digital circuit.

Claim 2 (original) A semiconductor integrated circuit, comprising:

an amplifier circuit of AM broadcast signals having a first P channel MOSFET for amplifying AM broadcast signals and a second P channel MOSFET cascade-connected to the first P channel MOSFET; and

a CMOS digital circuit; wherein

the first P channel MOSFET, the second P channel MOSFET and the CMOS digital circuit are formed on the same circuit board by a CMOS process.

Claim 3 (original) A semiconductor integrated circuit, comprising:

an amplifier circuit of AM broadcast signals having a first P channel MOSFET for amplifying AM broadcast signals and a bias circuit for giving a specific bias to the first P channel MOSFET; and

a CMOS digital circuit; wherein

the first P channel MOSFET, the bias circuit and the CMOS digital circuit are formed on the same circuit board by the CMOS process.

Claim 4 (original) A semiconductor integrated circuit, comprising;

an amplifier circuit of AM broadcast signals having a first P channel MOSFET for amplifying AM broadcast signals, a second P channel MOSFET cascade-connected to the first P channel MOSFET and a bias circuit for giving a specific bias to the first P channel MOSFET; and

a CMOS digital circuit, wherein

the first P channel MOSFET, the second P channel MOSFET, the bias circuit and the CMOS digital circuit are formed on the same circuit board by the CMOS process.

Claim 5 (currently amended) The semiconductor integrated circuit according to claim 1[, 2, or 4], which has an AGC circuit for controlling the amplification degree of the second P channel MOSFET.

6. (currently amended) The semiconductor integrated circuit according to claim 2[, 3, 4, or 5], wherein

the bias circuit has the third MOSFET which together with the first P channel MOSFET constitutes a current mirror circuit.

7. (original) The semiconductor integrated circuit according to claim 6, wherein

the bias circuit has the third MOSFET which together with the first P channel MOSFET constitutes a current mirror circuit, and makes the ratio of the channel width of the third MOSFET to the channel width of the first P channel MOSFET 1 : k ($k \geq 1$).

8. (currently amended) The semiconductor integrated circuit according to claim 6 [or 7], wherein

the bias circuit is constituted in such a way that one end of either the drain or the source is connected to a power-supply voltage, the other end of either the drain or the source is connected to the constant-current power supply, and the gate is connected to the constant-current power supply.

9. (original) A method of manufacturing a semiconductor integrated circuit which forms a first P channel MOSFET for amplifying AM broadcast signals and a second P channel MOSFET cascade-connected to the first P channel MOSFET, and a CMOS digital circuit on the same circuit board by the CMOS process.

10. (original) The method of manufacturing a semiconductor integrated circuit, wherein

an AGC circuit for controlling the amplification degree of the second P channel MOSFET is provided.

11. (original) The method of manufacturing a semiconductor integrated circuit according to claim 9, which forms the third MOSFET and the second P channel MOSFET constituting a current mirror circuit, and which makes the ratio of the channel width of the third MOSFET to the channel width of the first P channel MOSFET 1 : k ($k \geq 1$).

12. (new) The semiconductor integrated circuit according to claim 2, which has an AGC circuit for controlling the amplification degree of the second P channel MOSFET.

13. (new) The semiconductor integrated circuit according to claim 4, which has an AGC circuit for controlling the amplification degree of the second P channel MOSFET.

14. (new) The semiconductor integrated circuit according to claim 3, wherein

the bias circuit has the third MOSFET which together with the first P channel MOSFET constitutes a current mirror circuit.

15. (new) The semiconductor integrated circuit according to claim 4, wherein

the bias circuit has the third MOSFET which together with the first P channel MOSFET constitutes a current mirror circuit.